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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/604,474	07/24/2003	Tz-Jang Tseng	10879-US-PA	1473

31561 7590 12/14/2004

JIANQ CHYUN INTELLECTUAL PROPERTY OFFICE
7 FLOOR-1, NO. 100
ROOSEVELT ROAD, SECTION 2
TAIPEI, 100
TAIWAN

EXAMINER	
NORRIS, JEREMY C	

ART UNIT	PAPER NUMBER
2841	

DATE MAILED: 12/14/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/604,474	TSENG ET AL.	
	Examiner	Art Unit	
	Jeremy C. Norris	2841	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 July 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Priority

Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Drawings

The drawings are objected to because the sectional views are not properly cross-hatched (see MPEP 608.02). Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

Applicant is reminded of the proper content of an abstract of the disclosure.

A patent abstract is a concise statement of the technical disclosure of the patent and should include that which is new in the art to which the invention pertains. If the patent is of a basic nature, the entire technical disclosure may be new in the art, and the abstract should be directed to the entire disclosure. If the patent is in the nature of an improvement in an old apparatus, process, product, or composition, the abstract should include the technical disclosure of the improvement. In certain patents, particularly those for compounds and compositions, wherein the process for making and/or the use thereof are not obvious, the abstract should set forth a process for making and/or use thereof. If the new technical disclosure involves modifications or alternatives, the abstract should mention by way of example the preferred modification or alternative.

The abstract should not refer to purported merits or speculative applications of the invention and should not compare the invention with the prior art.

Where applicable, the abstract should include the following:
(1) if a machine or apparatus, its organization and operation;
(2) if an article, its method of making;
(3) if a chemical compound, its identity and use;
(4) if a mixture, its ingredients;
(5) if a process, the steps.

Extensive mechanical and design details of apparatus should not be given.

Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

The abstract of the disclosure is objected to because of the use of the phrase "The present invention provides". Correction is required. See MPEP § 608.01(b).

Claim Objections

Claims 8, 13, and 14 are objected to because of the following informalities: Regarding claims 8 and 14, both claims state the limitation "a third dielectric layer filled with the space". Since a "space" cannot "fill" anything, Examiner assumes this is a typo and Applicant intended to state --filled *within* the space--. This is the interpretation the Examiner has used for examination on the merits. Regarding claim 13, change "anda second bonding pad" --and a second bonding pad--. Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-7 and 9-12 are rejected under 35 U.S.C. 102(e) as being anticipated by US 6,414,248 (hereafter Sundstrom).

Sundstrom discloses, referring to figures1-5, an inner layer structure of a circuit board, comprising; a dielectric layer (12) having a first side and a second side; a first

bonding pad (20) on said first side of said dielectric layer; a first bump (30), wherein one end of said first bump is connected to said first bonding pad; a second bonding pad (22) on said second side of said dielectric layer; and a second bump (30), wherein one end of said second bump is connected to said second bonding pad [claim 1], further comprising a first circuit pattern (14) on said first side of said dielectric layer forming said first bonding pad [claim 2], further comprising a second circuit pattern (15) on said second side of said dielectric layer forming said second bonding pad [claim 3].

Similarly, Sundstrom discloses, referring to figures 1-5, an inner layer structure of a circuit board, comprising; a dielectric layer (12) having a first side and a second side, wherein said dielectric layer includes a through hole (16) penetrating through said dielectric layer and said through hole connects said first side and said second side of said dielectric layer; a conducting plug within said through hole (see col. 3, lines 45-55); and a bump (30), wherein one end of said bump is connected to an end of said conducting plug near said first side (see col. 3, lines 45-55) [claim 4], wherein said conducting plug includes a conducting wall (34) on the inner side wall of said first through hole and said conducting wall extends to said first side of said dielectric layer, and a portion of said conducting wall extending to said first side of said dielectric layer forms a ring pad, wherein one end of said bump is connected to said ring pad (see figures 4-5) [claim 5], wherein said conducting plug includes a conducting column (see col. 3, lines 45-55) [claim 6].

Additionally, Sundstrom discloses, an inner layer structure of a circuit board, comprising; a dielectric layer (12) having a first side and a second side, wherein said

dielectric layer includes a through hole (16) penetrating through said dielectric layer and said through hole connects said first side and said second side of said dielectric layer; a conducting plug within said through hole (see col. 3, lines 45-55); a second dielectric layer (32) having a third side (see col. 3, lines 40-45); a bonding pad on said third side of said second dielectric layer; and a bump, wherein one end of said bump is connected to said bonding pad (see col. 3, line 55 – col. 4, line 10) and another end of said bump is connected to an end of said conducting plug near said second side of said first dielectric layer (see col. 3, lines 45-55) [claim 7], wherein said conducting plug includes a conducting wall (34) on the inner side wall of said first through hole and said conducting wall extends to said second side of said first dielectric layer, and a portion of said conducting wall extending to said second side of said first dielectric layer forms a ring pad, wherein another end of said bump is connected to said ring pad (see figures 4-5) [claim 9], wherein said conducting plug includes a conducting wall (34) on the side wall of said through hole and the inner side of said conducting wall surrounds a second through hole, and one end of said bump is embedded in said second through hole and is connected to an inner side of said conducting wall near said first side of said first dielectric layer (see figure 4) [claim 10], wherein said conducting plug includes a conducting column (see col. 3, lines 45-55) [claim 11], further comprising a circuit pattern on said third side of said second dielectric layer forming said bonding pad (see col. 3, line 65 – col. 4, line 10) [claim 12].

Claims 7 and 8 are rejected under 35 U.S.C. 102(e) as being anticipated by US 6,711,025 (hereafter Ho).

Ho discloses, an inner layer structure of a circuit board, comprising; a dielectric layer (40) having a first side and a second side, wherein said dielectric layer includes a through hole (41) penetrating through said dielectric layer and said through hole connects said first side and said second side of said dielectric layer; a conducting plug within said through hole (43); a second dielectric layer (30) having a third side; a bonding pad (32) on said third side of said second dielectric layer; and a bump (32), wherein one end of said bump is connected to said bonding pad and another end of said bump is connected to an end of said conducting plug near said second side of said first dielectric layer [claim 7], further comprising a third dielectric layer (44) filled within the space between said first dielectric layer and said second dielectric layer [claim 8].

Claims 13-17 are rejected under 35 U.S.C. 102(e) as being anticipated by US 6,822,169 (hereafter Kataoka).

Kataoka discloses, referring to figure 7, an inner layer structure of a circuit board, comprising: a first dielectric layer (11) having a first side; a first bonding pad (4) on said first side of said first dielectric layer; a first bump (9a), wherein one end of said first bump is connected to said first bonding pad; a second dielectric layer (14) having a second side; and a second bonding pad (7) on said second side of said second dielectric layer; wherein said second bonding pad is connected to another end of said first bump [claim 13], further comprising a third dielectric layer (13) filled within the

space between said first dielectric layer and said second dielectric layer [claim 14], further comprising a second bump (8), wherein the one end of said second bump is connected to said second bonding pad, and said second bonding pad is indirectly connected to another end of said first bump via said second bump [claim 15], further comprising a first circuit pattern (3) on said first side of said first dielectric layer forming said first bonding pad [claim 16], further comprising a second circuit pattern (6) on said second side of said second dielectric layer forming said second bonding pad [claim 17].

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The following documents disclose PCB interconnections:

US 5,691,041	Frankeny et al.,
US 6,329,827	Beaman et al.,
US 6,354,844	Coico et al.,
US 2003/0143872	Keller.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jeremy C. Norris whose telephone number is 571-272-1932. The examiner can normally be reached on Monday - Friday, 9:30 am - 5:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamand Cuneo can be reached on 571-272-1957. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JCSN

HAMAND CUNEO
SUPERVISORY PATENT EXAMINER
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